AMENDMENTS TO THE SPECIFICATION

The following is a marked up version of each replacement paragraph and/or section of the specification in which underlines indicate insertions and strikethrough or double brackets indicate deletions.

Please replace paragraph **[0016]** with the following paragraph:

[0016] The clock signal generator 200 generates first, second and third clock signals (clock1, clock2, clcok3). The level shifter 210 changes a level of the input voltage V_{DD} in response to the first clock signal clock1 to generate a switching ~~control signal .~~control signal. The reference signal generator 220 generates a reference voltage (Vref) representing the desired boosted voltage. The voltage divider 230 divides boosted voltage Vout to generate a divided voltage (Vd) representing the boosted voltage Vout. The amplifier 240 amplifies a difference voltage between the reference voltage Vref and the divided voltage Vd to generate a control voltage (Vctrl). The voltage controlled current source 250 generates the control current Ictrl based on the control voltage Vctrl. The apparatus for controlling the boosted voltage is connected to a load 260 such as a capacitor C and a resistor R connected in parallel to the capacitor C. The boosted voltage Vout is provided to the load 260.

Please replace paragraph **[0019]** with the following paragraph:

[0019] As shown in Fig. [[3]] 2, in one exemplary ~~embodiment ,~~embodiment, the amplifier 240 may be a differential amplifier. An inverting (-) terminal of the differential amplifier 240 receives the reference voltage Vref, and a non-inverting (+) terminal of the differential amplifier 240 receives the divided voltage Vd.

Please replace paragraph **[0020]** with the following paragraph:

[0020] In the exemplary embodiment of Fig [[3]] 2, the VCCS 250 includes a first PMOS transistor MP1. A control electrode of the first PMOS transistor MP1 receives the output voltage of the differential amplifier 240, a first current electrode of the first PMOS transistor MP1 receives the input voltage V_{DD}, and a second current electrode of the first PMOS transistor MP1 is connected to the first switch S1.

Please replace paragraph **[0027]** with the following paragraph:

[0027] The clock signal generator 200 generates the first, second and third clock signals clock1, clock2, clock3. Fig. 3 illustrates an exemplary embodiment of the first, second and third clock signals clock1, clock2, clock3 generated by the clock signal generator 200. As ~~shown ,~~shown, the first clock signal clock1 repeats a high level and a low level with a fixed period. A front edge of the second clock signal clock2 is delayed by a fixed time Δt with respect to a front edge of the first clock signal clock1, and the high level period of the second clock signal clock2 is shorter than that of the first clock signal clock 1 such that the high level of a pulse in the second clock signal clock2 ends before the high level of a corresponding pulse in the first clock signal clock1. The third clock signal clock3 is an inverse of the first clock signal clock1.